Examiner J. Maldonado is thanked for the thorough examination and search of the subject Patent Application. Claims 1 and 9 have been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Please enter Amended Claims 1 and 9 as preliminary amendments to the subject Patent Application under Continuing Examination. Applicant asks that the Examiner consider the following remarks regarding the Examiner's finding of a rejection of Claims 1-23 under 35 U.S.C. 103(a) during the preceding examination.

Reconsideration of the rejection of Claims 1-23 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,693,568 to Liu et al in view of U.S. Patent 6,080,660 to Wang et al based on Amended Claims 1 and 9 the following remarks.

Applicant has amended Claims 1 and 9 to remove the limitation, added during previous amendment, of the use of a timed etch during the etching step to form vias. In particular, Amended Claim 1 now reads:

1. (AMENDED) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a metal layer overlying said semiconductor substrate;

etching through said metal layer to form connective lines;

thereafter etching partially through said metal layer to form vias [using a timed etch];

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

This amendment returns Amended Claims 1 and 9 to their original form.

Applicant has carefully reviewed the cited art and has found that Liu and Wang do not teach nor suggest a critical element of Applicant's invention. In particular, Applicant

teaches (for example in Claim 1, lines 6-12 and in Figs. 4-7) forming the interconnect structure by (1) etching through the entire metal stack (first metal 58, etching stop 62, second metal 66, and ARC 70) to form the interconnect lines, THEN (2) partially etching through metal stack (ARC 70 and second metal 66) to form vias, and THEN (3) depositing a dielectric layer to fill the spaces between the metal structures. Note that this sequence is made explicit by the "thereafter" form of lines 8 and 10. Further, Applicant notes that, in the original Specification, on page 14, the following notation is made: "Note that, since the dielectric layer 90 does not experience metal etching, cleaning, or photoresist stripping processes, no poisoning or bowing is seen." It is, therefore, a critical feature of the present invention to form the metal interconnects using a sequence where the dielectric layer is added after the metal etching steps.

Referring now to Liu, in Fig. 2, the metal stack 7, 8, 9 is etched through such that the metal lines are formed in layer 7. In Fig. 3, however, the dielectric layer 30 is "deposited to fill spaces formed by removing portions of the three-layer sandwich and planarized to form second dielectric 30 and to expose remaining portions of second conductive layer 9." (column

7, lines 23-27) This is especially significant because, in the next steps, a "resist mask 31" is applied and used to mask the partial metal etch step which etches through only layer 9 as shown in Fig. 4. This observation is important for two reasons. First, Liu clearly teaches a different method of forming the interconnects because the sequence is (1) etch though metal stack, (2) deposit dielectric fill, and (3) etch through top metal layer as opposed to Applicant's Claimed invention featuring the sequence: (1) etch through metal stack, (2) etch through top metal layer, and (3) deposit dielectric fill. Second, Liu's method therefore exposes the dielectric layer 30 to both the metal etch process and the photoresist strip process to remove the resist mask 31. Again, Applicant clearly states in the Specification, page 14, that the novel sequence of steps taught by the Applicant is used to specifically avoid this exposure.

Referring now to Wang, in Fig. 2A, the metal layer 22 and 24 is etched through. Next, in Fig. 2b, the dielectric layer 23 is deposited to fill the gaps between the etch metal lines 22 and 24. Finally, in Fig. 2C, the metal layer 22 and 24 is partially etched with the dielectric layer 23 in place. Again, this sequence of (1) etch though metal stack, (2) deposit

dielectric fill, and (3) partially etch through metal layer is opposed to Applicant's Claimed invention featuring the sequence: (1) etch through metal stack, (2) etch through top metal layer, and (3) deposit dielectric fill.

From this analysis, it is seen that Liu, Wang, and the combination of Liu and Wang, do not teach nor suggest a key part of Applicant's Claimed invention. It would not have been obvious to one skilled in the art at the time of the invention to practice Applicant's Claimed invention based on the teachings of Liu in view of Wang. Therefore, Applicant respectfully requests that the rejection of Claims 1-23 rejected under 35 U.S.C. 103(a) be reconsidered under continuing examination.

Reconsideration of the rejection of Claims 1-23 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,693,568 to Liu et al in view of U.S. Patent 6,080,660 to Wang et al based on Amended Claims 1 and 9 the above remarks.

Applicant have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

It is requested that should Examiner J. Maldonado not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

Douglas R. Schnabel, Reg. No. 47,927

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend Claim 1 as follows:

1. (AMENDED) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a metal layer overlying said semiconductor substrate;

etching through said metal layer to form connective lines;

thereafter etching partially through said metal layer to form vias [using a timed etch];

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

Please amend Claim 9 as follows:

9. (AMENDED) A method of forming self-aligned, anti-via

interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing a second metal layer overlying said first metal layer;

depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;

etching through said anti-reflective coating layer, said second metal layer, and said first metal layer to form connective lines;

thereafter etching through said anti-reflective coating layer and said second metal layer to form vias [using a timed etch];

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.